CARBON NANOTUBE THIN FILM TRANSISTORS BASED ON AEROSOL METHODS

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We demonstrate a fabrication method of high-performance field-effect transistors (FETs) based on dry-processed random single-walled carbon nanotube networks (CNTNs) deposited at room temperature. This method is an advantageous alternative to solution processed and direct CVD grown CNTN FETs, which allows using various substrate materials (including heat intolerant plastic substrates) and enables an efficient, density controlled, scalable deposition of as produced single-walled CNTNs directly from the aerosol (floating catalyst) synthesis reactor [1]. Two types of thin film transistor (TFT) structures were fabricated to evaluate the FET performance of dry-processed CNTNs: bottom-gate transistors on Si/SiO₂ substrates and top-gate transistors on polymer substrates (see Figure 1). Devices exhibited on/off ratios up to 10⁵ and field-effect mobilities up to 4 cm²/Vs. The suppression of hysteresis in the bottom-gate device transfer characteristics by means of passivation with an atomic layer deposited Al₂O₃ film was investigated. A 32 nm thick Al₂O₃ layer was found to be able to eliminate the hysteresis [2].

Figure 1. Schematics of a typical bottom-gate (a) and top-gate (b) CNTN FET structures.